AMENDMENTS TO THE SPECIFICATION:

In The Specification:

Please replace the paragraph beginning at page 11, line 3, with the following:

Referring now to the drawings, and more particularly to FIG. 1, there is shown a high level schematic block diagram of a basic form of the personality compiler in accordance with the invention and connected to provide state tables to a finite state machine (FSM) in a device, preferably a hardware parsing accelerator. Initially, it should be noted that the personality compiler 100 can be implemented as a stand-alone device which can be connected to a memory 105 (e.g. with a hardware parser accelerator off-line) which can then be accessed to obtain a state transition specification to be loaded, when needed on an on-demand basis, into the state tables (112) of an FSM by a loader 110 or integrated with a FSM 140 in an arbitrary device (indicated by dashed line 120) to be partially or wholly controlled thereby, allowing the personality of the device to be updated in real time or substantially so. (It should be appreciated in this latter case, that the operation of the invention in substantially real time, particularly by accelerating real-time operation through compiling an alternate version of a language grammar specification, allows it to adapt over time to patterns and conditions encountered in the input stream(s); thus providing a rudimentary learning capability in the personality compiler as well as in the device including the FSM. By the same token, it should be appreciated that parts of the process which will be described below and which yield intermediate results, such as preprocessing of the grammar specification (102) (e.g. up to step 250 of FIG. 2B or to provide pre-generated state tables which are archivally stored) may be operated in a stand-alone fashion and the processing continued from stored data (e.g. finite automata or state tables) when needed. The preferred application and environment of the invention is in connection with a hardware accelerator as depicted by dashed line 130 in either an integrated or a wholly or partially stand-alone configuration.

Please replace the paragraph beginning at page 12, line 11, with the following:

Regardless of the implementation of the invention, it will be useful to an understanding of the invention to review the nature of a state table for a FSM, particularly in regard to the preferred environment of a hardware parser accelerator. Three different implementations of hardware parser accelerators are respectively disclosed in U.S. patent applications Ser. Nos. 10/331,315 , 10/331,879 and 10/334,086 ~~10/_______, _______, 10/_______, _______ and 10/_______, _______~~(Attorney's Docket Numbers FS-00766, FS-00767 and FS-00768) all filed on Dec. 31, 2002, and assigned to the assignee of the present invention and which are all hereby fully incorporated by reference. FIG. 2A illustrates a portion of an exemplary state table as disclosed therein.